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Patent

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1-29-02
Sulez

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	)	
	)	
McMahon	)	Examiner: Chambliss, A.
	)	
Serial No.:09/768,580	)	Art Unit: 2814
	)	
Filed: January 23, 2001	)	
	)	
For: METHOD OF FABRICATING A STACKED CHIP PACKAGE	)	
	)	

Box Non-Fee Amendment
Commissioner for Patents
Washington, D.C. 20231

AMENDMENT AND RESPONSE TO OFFICE ACTION

Sir:

In response to the Office Action mailed August 13, 2001, Applicant respectfully requests the Examiner to enter the following amendment and to consider the following remarks.

Certificate of Mailing

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to Box Non-Fee Amendment, Commissioner for Patents, Washington, D. C. 20231
on November 13, 2001
(Date of Deposit)

Dianne Neathery
(Typed or printed name of person mailing correspondence)

Dianne Neathery
Signature

11-13-01
Date

IN THE CLAIMS:

Below is submitted a clean version of the entire set of pending claims per 37 CFR §1.121(c)(3).

21. (amended) A method of constructing a multi-chip package, comprising:

placing a first chip package on a first shelf;

electrically attaching said first chip package to a plurality of shelves;

placing a second chip package on a second shelf wherein said second shelf is stacked above said first shelf; and

electrically attaching said second chip package to said second shelf.

22. (amended) The method of claim 21 further comprising the step of filling said multi-chip package above said second chip package with an encapsulant.

23. (amended) The method of claim 22 wherein said step of placing said second chip package on said second shelf further comprises placing said second chip package on said second shelf with a sealer such that a sealed open cavity below said second shelf protects said first chip package.

24. (amended) The method of claim 21 wherein said step of placing said first chip package further comprises placing a CPU chip package on said first shelf.

25. (amended) The method of claim 21 wherein said step of placing said second chip package further comprises placing a memory cache on said second shelf.

26. (amended) The method of claim 21 wherein said step of electrically attaching said first chip package further comprises wire bonding said first chip package to said plurality of shelves.

27. (amended) The method of claim 21 wherein said step of electrically attaching said second chip package further comprises wire bonding said second chip package to said plurality of shelves.

IN THE SPECIFICATION

The applicant has accepted the Examiner's suggested new title to the application, "METHOD OF FABRICATING A STACKED CHIP PACKAGE"

Please replace the paragraph on page 13, beginning on line 18 of the specification with the following paragraph:

The SRAM cache 74 is mounted to a ceramic substrate 32 through use of solder balls 72 (step 78). A standard flip chip substrate may be used for the SRAM cache 74. An underfill coating (not shown) may be applied (step 80) to further secure the SRAM cache 74 to the substrate 32, a functionality test is performed to verify performance of the SRAM chip (step82). If the SRAM chip is satisfactory, fabrication of the multi-chip package 70 may continue, otherwise the SRAM chip will be replaced.

Please replace the paragraph on pages 14 – 15, beginning on page 14, line 18 of the specification with the following paragraph:

The multi-chip package 90 can be fabricated in a similar process flow as that discussed above with respect to multi-chip package 70. A CPU die 26 is first attached to a slug 24 (step 98). The slug 24 supporting the CPU die 26 is then attached to the organic package 93, where the CPU die 26 is electrically connected to the package 93 via wire bonds I 28 and 30 (step 100). Note that the organic package 93 is comprised of a series of layers or shelves 14, 16, 18, 20, and 22, and has connector pins 94 staked through (or extending through) the package 93 to allow the multi-chip package 90 to be electrically coupled to other devices (e.g., a PCB). Once the CPU die 26 and slug 24 are attached to the chip package 17, a first encapsulant fills (step 102) the area 92 above the CPU die 26. The encapsulant (not shown) is generally an epoxy used for environmental protection of the die 26.

Please replace the last paragraph on page 17 beginning on line 7 of the specification with the following paragraph:

Once any testing is complete, a CPU device 140 is mounted to the base of the package 93 and electrically connected through use of the solder balls 142. Note that ceramic package 17 is comprised of a series of layers or shelves 14, 16, 18, 20, and 22, and has solder balls 122 attached to the surface of the upper shelf 14 to allow the multi-chip package 120 to be electrically coupled to other devices (e.g., a PCB). In this manner, the multi-chip package 118 may be used to mount a plurality of semiconductor devices to, for example, a PCB in a single chip footprint. Standard single package PGA and BGA options have not been capable of supporting multi-chip formats without expanding the footprint of the package. Thus, the present invention provides significant advantages over the prior art.

STATUS OF CLAIMS

Claims 21 – 27 are pending and the Examiner has rejected claims 21 - 27.

REMARKS

37 CFR §1.84(p)(5) drawing objections

The Examiner has objected to the drawings as failing to comply with 37 CFR §1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: 38, 52, 80, 102, 120, 122, 130, and 134. Correction is required.

The Applicant has amended the specification to reference figure callouts 80, 102, and 122 and asserts that no new matter has been added to the specification. In particular to the paragraph replaced on page 17 beginning on line 7 of the specification, the Applicant's newly added wording is taken from page 14, a sentence beginning on line 22. This sentence, beginning with the wording "Note that the organic package 93....", references connector pins 94, which are also reflected in Fig. 7. It can be seen that the solder balls 122 in Fig. 7 serve the same

function as the connector pins 94 in Fig. 7 and so addition of this wording does not constitute new matter

Applicant has noted Examiner's objection of figures for callouts 38, 52, 120, 130 and 134 failing to be referenced in the disclosure. A review of the application by Applicant has found callout 38 on page 12, line 23, callout 52 on page 13, line 15, callout 120 on page 16, line 5, callout 130 on page 16, line 6, and finally callout 134 on page 16, line 16. As a result, Applicant has not amended the specification with regard to these noted callouts.

35 USC §112, Second Paragraph rejections

The Examiner has rejected claims 23 - 25 under 35 USC §112, second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Applicant has amended claims 23 – 25 to correct these antecedent problems cited by the Examiner to more particularly point out and distinctly claim the subject matter which Applicant regards as the invention.

35 USC §102(b) rejections

The Examiner has rejected claims 21, 26, and 27 under 35 USC §102(b) as being anticipated by Kiyoshi (JP 4-219966).

The Examiner states that with respect to Claim 21, *Kiyoshi* places a first chip package 4 on a first shelf, which is electrically attached to the first shelf. A second chip package 4 (i.e. the chip above the first chip package) is electrically attached to the second shelf (see English abstract and figures).

Applicant claims in amended claim 21, "...placing a first chip package on a first shelf; electrically attaching said first chip package to a plurality of shelves ..." Claim 21 claims wiring the first chip package to a plurality of shelves within the multi-chip package. This amendment is supported by Applicant's FIGS. 1, 3, and 5 where it is shown wiring elements 28 and 30 from the first chip package are attached to shelf 22 and to shelf 20. Applicant has amended claims 22 – 27 to be consistent

with amended claim 21. Applicant asserts that no new matter has been placed in the amended claims.

Applicant further submits that in as much as claims 26 and 27 depend from claim 21, they include all the limitations of that independent claim. Therefore, claims 26 and 27 are thought allowable for at least the same reasons as claim 21.

35 USC §1.03(a) rejections

Applicant submits that in as much as claims 22 – 25 depend from claim 21, they include all the limitations of that independent claim. Therefore, claims 22 – 25 are thought allowable for at least the same reasons as claim 21.

It is respectfully submitted, that in view of the amended application title, amended specification paragraphs, amended claims, and the remarks set forth herein, all requests by the Examiner have been met and all rejections and objections overcome.

Authorization is hereby given to charge our Deposit Account No. 02-2666 for any charges that may be due. Furthermore, if an extension is required, then Applicant hereby requests such an extension.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN

Dated: 11/13, 2001

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